

**PATENT APPLICATION**

Sheet 1 of 3

<b>FORM PTO-1449</b>  <b>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT</b>  (Use several sheets if necessary)	ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
	200313751-1		
	APPLICANT		
	Gregory Edward Tierney, et al.		
	FILING DATE	GROUP	
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**REFERENCE DESIGNATION U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
/MR/	1A	2001/0034815	10/25/2001	Dungan, et al.	
/MR/	1B	2002/0009095	01/24/2002	Van Doren, et al.	
/MR/	1C	2002/0073071	06/13/2002	Pong, et al.	
/MR/	1D	2003/0018739	01/23/2003	Cypher, et al.	
/MR/	1E	2002/0144063	10/03/2002	Peir, et al.	
/MR/	1F	2003/0140200	07/24/2003	Jamil, et al.	
/MR/	1G	2003/0145136	07/31/2003	Tierney, et al.	
/MR/	1H	2003/0195939	10/16/2003	Edirisooriya, et al.	
/MR/	1I	2003/0200397	10/23/2003	McAllister, et al.	
/MR/	1J	5,355,467	10/11/1994	MacWilliams, et al.	
/MR/	1K	5,802,577	09/01/1998	Bhat, et al.	

**FOREIGN PATENT DOCUMENTS**

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
/MR/	1L	EP 1 162 542	12.12.2001	Agere Systems		
	1M					
	1N					
	1O					
	1P					

**OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)**

/MR/	1Q	RAJEEV, JOSHI, et al., "Checking Cache-Coherence Protocols with TLA+", Kluwer Academic Publishers, 2003, pp. 1-8
/MR/	1R	MARTIN, MILO M.K., et al., "Token Coherence: Decoupling Performance and Correctness", ISCA-30, pp. 1-12, June 9-11, 2003
/MR/	1S	ACACIO, MANUEL E., et al., "Owner Prediction for Accelerating Cache-to-Cache Transfer Misses in a cc-NUMA Architecture", IEEE 2002

EXAMINER  
/Midys Rojas/ (06/23/2007)

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**REFERENCE DESIGNATION U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
/MR/	2A	5,829,040	10/27/1998	Son	
/MR/	2B	5,875,467	02/23/1999	Merchant	
/MR/	2C	5,875,472	02/23/1999	Bauman, et al.	
/MR/	2D	5,958,019	09/28/1999	Hagersten, et al.	
/MR/	2E	6,052,760	04/18/2000	Bauman, et al.	
/MR/	2F	6,055,605	04/25/2000	Sharma, et al.	
/MR/	2G	6,081,887	06/27/2000	Steely, Jr., et al.	
/MR/	2H	6,085,263	07/04/2000	Sharma, et al.	
/MR/	2I	6,108,737	08/22/2000	Sharma, et al.	
/MR/	2J	6,345,342 B1	02/05/2002	Arimilli, et al.	
/MR/	2K	6,356,918 B1	03/12/2002	Chuang, et al.	

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		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	2L					
	2M					
	2N					
	2O					
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**OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)**

/MR/	2Q	GHARACHORLOO, KOUROSH, et al., "Architecture and Design of AlphaServer GS320", Western Research Laboratory, (Date Unknown)
/MR/	2R	GHARACHORLOO, KOUROSH, et al., "Memory Consistency and Event Ordering in Scalable Shared-Memory Multiprocessors", Computer Systems Laboratory, pp. 1-14, (Date Unknown)
	2S	

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/MR/	3A	6,408,363 B1	06/18/2002	Lesartre, et al.	
/MR/	3B	6,457,100 B1	09/24/2002	Ignatowski, et al.	
/MR/	3C	6,457,101 B1	09/24/2002	Bauman, et al.	
/MR/	3D	6,490,661 B1	12/03/2002	Keller, et al.	
/MR/	3E	6,587,921 B2	07/01/2003	Chiu, et al.	
/MR/	3F	6,615,343 B1	09/02/2003	Talcott, et al.	
/MR/	3G	6,631,401 B1	10/07/2003	Keller, et al.	
/MR/	3H	6,633,970 B1	10/14/2003	Clift, et al.	
	3I				
	3J				
	3K				

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**OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)**

	3Q	
	3R	
	3S	

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